UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,981	07/18/2003	Christian May	P2001,0025	2995

24131 7590 02/23/2006

LERNER GREENBERG STEMER LLP
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,981	MAY ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 21* is/are rejected.

7)☒ Claim(s) *16-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-17 remain for examination. Claims 18-21 are newly presented.

2. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

3. The response filed on 12/14/05 by applicant will be addressed below to clarify the issue regarding the teaching of Chamber. Applicant argued that Chamber did not teach anything about the stack 306. In response, Examiner would like to point out that Chamber's stack 306 was shown to be connected to at least the control unit, the register bank (308), the auxiliary register (see auxiliary register valid bit register (310) (see fig.3). Therefore, it had storage capabilities.

Claims 1-17,21 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: no functional relation has been recited with respect the indication of the respective register containing the value with the stack buffer.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,9-12, 14,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamber (6,047,365) in view of Scheuneman (4,757,440) in view of Fitch et al. (5,056,060) .

4. As to claims 1,12,14,15, Chambers taught a microprocessor circuit, comprising'. at least :

a) one- control unit (300) (3121(316) ;

b) one memory (see fig.1C (16) for overall structure, see 5g.3 (306J) for free programming with at least one program having functions (see DRAM as system memory, it is free for programming because it is a system memory) , the memory connected to the control unit (see fig.3);

c) a stack (306) for buffer-storing data (see memory wave table sample page of 4-byte in col.5, lines 1-9) , the stack connected to the control unit;

d) a register bank having register (308) , the register bank connected to said control unit; and

e) an auxiliary register storing a number of bits (see valid bit register) , each of the bits belong associated with one of said registers of the register bank (see register bank 308) and indicating whether a respective one of the registers contained valid bit (see col.5, lines 28-46), the auxiliary register valid bit register 9310) connected to at least

one of the control unit, the register bank (308) , and a stack (306) .
The stack (306) connected to at least the control unit, the register bank (308), the auxiliary register (see auxiliary register valid bit register (310) .

5. As to the newly amended feature of "stack buffer", the stack buffer is being recited for storing the data of the auxiliary register or the register bank register, and no other functional relation has been recited with respect the indication of the respective register containing the value (see also the "112" above). Therefore, it is read as any stack buffer for storing data in general. Chamber did not specifically show his stack was used as a stack buffer for storing data of the auxiliary register or the register bank as claimed. However , Scheuneman disclosed a system including a stack buffer which included a tag bit for read and write operations (see col.18, lines 45-68, col.19, lines 1-51). It would have been obvious to one of ordinary skill in the art to use Scheuneman in Chamber for including the stack buffer for storing the data of the auxiliary register or the register bank as claimed because the use of Scheuneman could provide Chamber the ability to store the data of a predetermined register, such as register bank or auxiliary register, or the like, therefore, increasing the storage capacity of Chamber, and Chamber did taught a stack (306) , although whether the stack stored data of the auxiliary registry or the register bank was not shown, one of ordinary skill in the art should be able to recognize the stack of Scheuneman with the read/write tags could be used for Chamber's stack for storing data from the auxiliary register and register bank, and Chamber did taught the connection of his stack [306] with the auxiliary

register valid bit register (310) connected to at least one of the control unit and the register bank (308), which was a suggestion of the need for including the stack buffer for storing the data of the auxiliary register or the register bank for read and write purpose, and for doing so, provided a motivation.

6. Chamber did not specifically show his auxiliary register contained a value different from a logical "0'. as claimed. However, Fitch taught a logical 1 for a valid determination (see col.15, lines 40-45, see the logical '11" as valid signal). It would have been obvious to one of ordinary skill in the art to use Fitch in Chambers for including a value different from logical "0.. (i.e. logical 1'1") as claimed because the use of Fitch could provide the capability of Chamber to determine the validity of his register content based on the logic comparison, thereby minimizing the use of extra hardware overheads based on a single logical result, such as ("1" or "0"), and because although Chamber did not show how the logical determination was made, of ordinary skill in the and should be able to recognize Fitch's logical 1, Finch was different from logical "0" could be applicable for determine the valid bit of the register I order to provide logical comparison in Chamber. The examiner hold that the use of logical states , such as "0" or "1" should be well within the skill of ordinary in the art and applicable in many applications. Fitch is used to show the logical value could be used for a valid determination, and since Chamber already taught the valid determination, and since no specific application has been reflected into he claim, it provided a suggestion to

combined in order to provide the single comparison logical result, and in doing so, provided a motivation.

7. As to the last value on stack in claim 14, the auxiliary register of Chamber could be used in any order(see valid bit register .

8. As to claims 2,3, 4, Chamber also included further registers (see the greater and lesser number of registers in col.5, lines 40-47).

9. As to claim 5, Chamber's register was also in the same register bank (see fig.3(308)).

10. As to claims 9,10, Chamber also showed first and second areas (see the corresponding address space in 5g.3). As to the called function and both called function and calling functions, the examiner holds that Chamber's address space was applicable for storing any called function and calling function.

11. As to claim 11, Chamber also divided in sub areas (see portions (308) memory bank in fig.3).

12. Claims 6,7, 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamber (6,047,365) in view of Scheuneman (4,757,440) In view of Fitch et al. (5,056,060) as applied to claims 1 , 12 and further in view of Arnold et al. (4,558,176).

13. As to claims 6,7,8, neither Chamber, Scheuneman, nor Fitch specifically showed the accessible stack only to the operating system as claimed . However, Arnold disclosed a control stack inaccessible by external modifications (col.13, lines 28-44). It

should be understood that the stack not accessible by external modification, but it could be accessed by internal modifications, such as operating system of the system. It would have been obvious to one of ordinary skill in the art to use Arnold in Chamber for including the inaccessible stack as claimed because the use of Arnold could provide Chamber the ability to protect the content of his stack, and because Chamber taught a read only memory (see col.1, lines 16-32), which was not write accessible, and one of ordinary skill in the art should able to recognize the applicability of the system permission of either read, write or both in a memory in order to protect the content of the register bank for a particular application , and for above reasons , provided a motivation.

14. Claims 13, 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamber (6,047,365) in view of (4,757,440) in view of Fitch et al. (5,056,060) as applied to claim 12 and further in view of Wright ad al. (4,802,218).

15. As to claims 13, neither Chamber , Scheuneman , nor Fitch specifically show the permission of the data in the register bank as claimed. However, Wright disclosed a system for permitting readings of a memory section (see the locked memory section in Col.16, lines 60-65). It would have been obvious to one of ordinary a skill in the art to use Wright in Chamber for including the reading permission as clamed because Chamber taught a read only memory (see col.1, lines 16-32), which was not write accessible, and one of ordinary skill in the art should be able to recognize the

applicability of either read, write or both permissions in a memory in order to lock the data of the register bank for a specific application , and for above reasons , provided a motivation.

16. Claims 16, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Upon further review, none of the prior art of record further teaches the combined features of the circuit with a second stack for storing at least some data in the register bank and making the second stack inaccessible by a programmer and if the circuit changes from a first function to a second function, successively storing the data associated with the first function in the registers of the register bank and the bit sequence of the auxiliary register in one of the stack and the second stack.

17. Claims 18, 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches a register of the register bank is only stored on the stack if the associated bit of the auxiliary register has a value different from the logical "0".

18. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches a

register of the register bank is only stored on the stack if the associated bit of the auxiliary register has a value different from the logical "0".

19. Chamber (6,047,365), Fitch et al. (5,056,060 Wright et al. (4,802,218). And Arnold et al. (4,558,176) were cited on the record, therefore, copies are not being provided herein. Scheuneman (4,757,440) is a newly cited art.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or

the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan